

REMARKS

In response to the outstanding Office Action, claims 3, 10, 13, 22, 24, 32, 34, 36 and 45 have been amended, claims 23 and 33 have been canceled and new claims 47-57 have been added.

In the outstanding Office Action, the Examiner states that the reissue oath/declaration filed with the application is defective because it fails to identify at least one error which is relied upon to support the reissue application. The Examiner has also indicated that the reissue oath/declaration filed with the application is defective in that it fails to contain a statement that all errors that are being corrected in the reissue application arose without any deceptive intention on the part of the applicant. Enclosed herewith is an additional copy of the Reissue Application Declaration by the Inventor, as submitted concurrently with the application, with the relevant portions highlighted, indicating that both of these requirements were satisfied. It is respectfully requested that the rejection of the claims under 35 U.S.C. §251 be withdrawn.

Also in the outstanding Office Action, the Examiner indicates that the application was filed without the required offer to surrender the original patent. Enclosed herewith is a copy of the Offer to Surrender Patent by Assignee, as submitted concurrently with the application, as well as a copy of the return postcard indicating that the Offer to Surrender was

contained in the application package which was received by the Patent Office on February 8, 2001.

The examiner objected to the drawings, stating that the integrated circuit must be shown or the feature(s) canceled from the claim(s). However the examiner's attention is directed to the patent specification, column 2, lines 25-29, wherein it is stated:

"Also, as shown in the figure, the input voltage V_{in} is provided through resistor R_f to provide an analog voltage V for powering the analog devices in the integrated circuit, more specifically the circuit components within the heavier line in FIG. 2 encircling the elements of the integrated circuit itself."

(emphasis added)

Consequently, it is submitted that the integrated circuit is shown in the Figures. Accordingly, reconsideration of this objection is respectfully requested.

Submitted concurrently herewith are an Information Disclosure Statement, Form PTO/SB/08 and copies of cited references, with the appropriate fee, providing additional relevant prior art that has come to the attention of the applicant. Consideration of the references cited is respectfully requested. In addition, because of uncertainty in the

requirement, the Information Disclosure Statement includes art made of record in the original patent.

As the Examiner's Interview Summary shows, the undersigned held a telephonic interview with the Examiner on September 18, 2001 to discuss the independent claims in the application and the prior art relied upon by the Examiner, specifically, U.S. Patent No. 4,371,919 by Andrews et al. As the Examiner's Interview Summary indicates, the interview centered on the interleaved feature of the present invention in comparison to Andrews et al. In particular, the undersigned pointed out that in Andrews et al., multiple converters operate in parallel into a common load, the disclosure including a provision for distribution of the load evenly among the parallel converters. The converters themselves, however, each operate off their own RC timing circuit. In particular, Figure 3 of Andrews et al. of shows three converter circuits 131, 132 and 133 operating into a common node 104. Converter circuit 131 is shown in some detail, with additional converter circuits 132 and 133 shown only in a simple block form. Each converter circuit, such as converter circuit 131, has its own timing circuit comprised of resistor 54 and capacitor 56 (col. 3, starting on line 15), so that each converter circuit will operate at its own frequency without any synchronization between converter circuits, and of course therefore without any specific interleaving of the converter circuits. Consequently,

there is no fixed phase of operation between the converter circuits.

In the present invention, the operation of the converter circuits is intentionally synchronized so that the operation of the converter circuits is always interleaved, giving rise to various advantages, including reduced noise, reduced filtering requirements on the input and output of the converter, etc. In that regard, it was noted that in the two converter embodiment disclosed in the patent for which a reissue is sought, the two converters operate from a common clock (see the clock in Figure 2c of the patent), with the two converters being triggered out of phase with each other by the Q and the QB output of flip-flop 92.

In the interview with the Examiner, among the claims discussed in some detail was claim 1. It was pointed out that the interleaved nature of the converter circuit was expressly set forth in the preamble of the claim. In addition, however, the interleaved nature of the operation of the converters is also required in the body of the claim by the nature of the control circuits set forth therein. In particular, claim 1 includes the following limitation:

"the control circuits also being responsive to the difference in the voltage across the sense resistor when the first converter is drawing power from the power supply through the sense resistor and the second

converter is not, and when the second converter is drawing power from the power supply through the sense resistor and the first converter is not, to adjust the relative duty cycle of the first and second converters to tend to minimize the difference in the voltage across the sense resistor"

Inherent in this limitation is the interleaving referred to in the preamble. Accordingly, reconsideration of this rejection was and is requested.

Claim 10 was also discussed in the interview. As a result of that discussion, the undersigned has amended the claim to better set forth the interleaving claimed.

Amended claim 22 was also discussed, the undersigned pointing out that the body of the claim expressly requires "a plurality of pulse width modulators driven by a common oscillator in an interleaved manner" and "whereby the operation of the converter circuits is interleaved." Thus, the DC to DC switching circuit claimed is expressly limited to a plurality of pulse width modulators driven by a common oscillator (Andrews et al. discloses a separate oscillator for each converter) to provide interleaved operation of the pulse width modulators, and thus the converter circuits (Andrews et al. has parallel operation but not interleaved operation). It was also pointed out that the remaining independent claims also contain the express limitations

with respect to interleaving. Accordingly, reconsideration of the rejection of claims 1, 2, 9, 10 as now amended, 11, 12, 19-22, 30-32, 34 and 42-46 is respectfully requested.

In addition, new claims 47-50 have been added to claim the general invention in alternate terminology. Also, new claims 51-57 have been added which claim the same subject matter as claims 22, 32 and 46-50, respectively, though are expressly limited to buck converters. For the same reasons as set forth with respect to the other independent claims, it is believed that these claims are also allowable.

Accordingly, it is believed that all claims in the case are now in condition for allowance and therefore allowance at an early date is respectfully requested.

Version with Markings to Show Changes Made

IN THE CLAIMS:

Sub E3
BX
1 3. (Amended) The DC to DC switching circuit of claim 1
2 further comprised of an integrator having an output responsive to
3 the integral of an error signal, the error signal being
4 responsive to the voltage across the common load and a desired
5 voltage, the control circuits also being responsive to the output
6 of the integrator.

Sub D5
B2
1 10. (Amended) DC to DC switching circuit for controlling
2 power switching devices in a DC to DC converter having first and
3 second [interleaved] converter circuits operating into a common
4 load comprising:
5 a first pulse width modulator controlling the power
6 switching devices of the first converter circuit;
7 a second pulse width modulator controlling the power
8 switching devices of the second converter circuit;
9 a feedback circuit responsive to the voltage across the
10 common load;
11 control circuits for controlling the first and second pulse
12 width modulators responsive to the feedback circuit, the
13 operation of the first and second pulse width modulators being
14 interleaved;

15 the control circuits also being responsive to the difference
16 in current through the first converter and the second converter
17 to adjust the relative duty cycle of the first and second
18 converters to tend to minimize the difference in the voltage
19 across a [the] sense resistor;

20 [the current sense circuit,] the first pulse width
21 modulator, the second pulse width modulator, the feedback circuit
22 and the control circuits being in a single integrated circuit.

Sub 4
B3
1 13. (Amended) The DC to DC switching circuit of claim 12
2 further comprised of an integrator having an output responsive to
3 the integral of an error signal, the error signal being
4 responsive to the voltage across the common load and a desired
5 voltage, the control circuits also being responsive to the output
6 of the integrator.

Sub C1
B4
1 22. (Amended) A DC to DC switching circuit for controlling
2 power switching devices in a DC to DC converter having a
3 plurality of [interleaved] converter circuits operating into a
4 common load, comprising:

5 a plurality of pulse width modulators driven by a common
6 oscillator in an interleaved manner, each pulse width modulator
7 controlling power switching devices of one of the plurality of
8 [interleaved] converter circuits, whereby the operation of the
9 converter circuits is interleaved;

10 a feedback circuit responsive to a voltage across the common
11 load;
12 a voltage control circuit [circuits] for controlling the
13 plurality of pulse width modulators responsive to the feedback
14 circuit and a commanded output voltage [, and for adjusting a
15 nominal duty cycle of the plurality of interleaved converter
16 circuits]; and
17 a current balance control circuit for controlling the pulse
18 width modulators to balance the current in the plurality of
19 interleaved converter circuits;
20 the plurality of pulse width modulators and the control
21 circuits being in a single integrated circuit.

Sub C2
1 24. (Amended) The DC to DC switching circuit of claim 22
2 further comprised of an integrator having an output responsive to
3 the integral of an error signal, the error signal being
4 responsive to the voltage across the common load and a desired
5 voltage, the control circuits also being responsive to the output
6 of the integrator.

Sub C4
1 32. (Amended) A DC to DC switching circuit for controlling
2 power switching devices in a DC to DC converter having a
3 plurality of [interleaved] converter circuits operating into a
4 common load, comprising:

5 a plurality of pulse width modulators each controlling power
6 switching devices of one of the plurality of [interleaved]
7 converter circuits, the operation of the pulse width modulators
8 and the converter circuits being interleaved;

9 a feedback circuit responsive to a voltage across the common
10 load;

11 control circuits being responsive to the feedback circuit
12 and a commanded output voltage to control a nominal duty cycle of
13 the plurality of converter circuits, the control circuits also
14 adjusting a relative duty cycle of the plurality of converter
15 circuits to balance the current in the converter circuits;

16 the plurality of pulse width modulators and the control
17 circuits being in a single integrated circuit.

1 34. (Amended) The DC to DC switching circuit of claim 32
2 [33] wherein the control circuits control the plurality of pulse
3 width modulators.

1 36. (Amended) The DC to DC switching circuit of claim 35,
2 wherein the control circuits ~~[is]~~ are also responsive to the
3 output of the integrator.

1 45. (Amended) A circuit in a DC to DC converter having a
2 plurality of [interleaved] converter circuits operating into a
3 common load, comprising:

4 a plurality of pulse width modulators each controlling power
5 switching devices of one of the plurality of [interleaved]
6 converter circuits, the operation of the pulse width modulators
7 being interleaved;

8 control circuits for adjusting a nominal duty cycle of the
9 plurality of interleaved converter circuits;

10 the plurality of pulse width modulators and the control
11 circuits being in a single integrated circuit.

1 47. (New) A DC to DC switching circuit for controlling
2 power switching devices in a DC to DC converter having a
3 plurality of converter circuits operating into a common load,
4 comprising:

5 a plurality of pulse width modulators driven by a common
6 oscillator in an interleaved manner, each pulse width modulator
7 controlling power switching devices of one of the plurality of
8 converter circuits, whereby the operation of the converter
9 circuits is interleaved;

10 a feedback circuit responsive to a voltage across the common
11 load;

12 a voltage control circuit for controlling the plurality of
13 pulse width modulators responsive to the feedback circuit and a
14 commanded output voltage; and

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15 a current balance control circuit for controlling the pulse
16 width modulators to balance the current in the plurality of
17 interleaved converter circuits.

1 48. (New) A DC to DC switching circuit for controlling
2 power switching devices in a DC to DC converter having a
3 plurality of converter circuits operating into a common load,
4 comprising:

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5 a plurality of pulse width modulators each controlling power
6 switching devices of one of the plurality of interleaved
7 converter circuits, the operation of the pulse width modulators
8 and the converter circuits being interleaved;

9 a feedback circuit responsive to a voltage across the common
10 load;

11 control circuits responsive to the feedback circuit and a
12 commanded output voltage to control a nominal duty cycle of the
13 plurality of converter circuits, the control circuits also
14 adjusting a relative duty cycle of the plurality of converter
15 circuits to balance the current in the converter circuits.

1 49. (New) A circuit for a DC to DC converter having a
2 plurality of converter circuits operating into a common load,
3 comprising:

4 a plurality of pulse width modulators each controlling power
5 switching devices of one of the plurality of converter circuits,

6 the pulse width modulators being driven by a common oscillator
7 signal so that the operation of the pulse width modulators is
8 interleaved;

9 control circuits for adjusting a nominal duty cycle of the
10 plurality of interleaved converter circuits to control a voltage
11 on the common load, and for adjusting a relative duty cycle of
12 the plurality of converter circuits to balance the current in the
13 converter circuits.

B10 1 50. (New) A DC to DC switching circuit for controlling
2 power switching devices in a DC to DC converter having first and
3 second interleaved converter circuits operating into a common
4 load, comprising:

5 a first pulse width modulator controlling the power
6 switching devices of the first converter circuit;

7 a second pulse width modulator controlling the power
8 switching devices of the second converter circuit;

9 a feedback circuit responsive to the voltage across the
10 common load;

11 control circuits for controlling the first and second pulse
12 width modulators responsive to the feedback circuit;

13 the control circuits also being responsive to current
14 measurements through the first converter circuit and the second
15 converter circuit for adjusting the relative duty cycle of the
16 first and second converter circuits.

1 51. (New) A DC to DC switching circuit for controlling
2 power switching devices in a DC to DC converter having a
3 plurality of buck converter circuits operating into a common
4 load, comprising:

5 a plurality of pulse width modulators driven by a common
6 oscillator in an interleaved manner, each pulse width modulator
7 controlling power switching devices of one of the plurality of
8 buck converter circuits, whereby the operation of the buck
9 converter circuits is interleaved;

10 a feedback circuit responsive to a voltage across the common
11 load;

12 a voltage control circuit for controlling the plurality of
13 pulse width modulators responsive to the feedback circuit and a
14 commanded output voltage; and

15 a current balance control circuit for controlling the pulse
16 width modulators to balance the current in the plurality of
17 interleaved buck converter circuits;

18 the plurality of pulse width modulators and the control
19 circuits being in a single integrated circuit.

1 52. (New) A DC to DC switching circuit for controlling
2 power switching devices in a DC to DC converter having a
3 plurality of buck converter circuits operating into a common
4 load, comprising:

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a plurality of pulse width modulators each controlling power
switching devices of one of the plurality of buck converter
circuits, the operation of the pulse width modulators and the
buck converter circuits being interleaved;

a feedback circuit responsive to a voltage across the common
load;

control circuits being responsive to the feedback circuit
and a commanded output voltage to control a nominal duty cycle of
the plurality of buck converter circuits, the control circuits
also adjusting a relative duty cycle of the plurality of buck
converter circuits to balance the current in the buck converter
circuits;

the plurality of pulse width modulators and the control
circuits being in a single integrated circuit.

53. (New) A DC to DC switching circuit for controlling
power switching devices in a DC to DC converter having first and
second interleaved buck converter circuits operating into a
common load, comprising:

a first pulse width modulator controlling the power
switching devices of the first buck converter circuit;

a second pulse width modulator controlling the power
switching devices of the second buck converter circuit;

a feedback circuit responsive to the voltage across the
common load;

11 control circuits for controlling the first and second pulse
12 width modulators responsive to the feedback circuit.

13 the control circuits also being responsive to current
14 measurements through the first buck converter circuit and the
15 second buck converter circuit for adjusting the relative duty
16 cycle of the first and second buck converter circuits;

17 the first pulse width modulator, the second pulse width
18 modulator, the feedback circuit and the control circuits being in
19 a single integrated circuit.

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1 54. (New) A DC to DC switching circuit for controlling
2 power switching devices in a DC to DC converter having a
3 plurality of buck converter circuits operating into a common
4 load, comprising:

5 a plurality of pulse width modulators driven by a common
6 oscillator in an interleaved manner, each pulse width modulator
7 controlling power switching devices of one of the plurality of
8 buck converter circuits, whereby the operation of the buck
9 converter circuits is interleaved;

10 a feedback circuit responsive to a voltage across the common
11 load;

12 a voltage control circuit for controlling the plurality of
13 pulse width modulators responsive to the feedback circuit and a
14 commanded output voltage; and

15 a current balance control circuit for controlling the pulse
16 width modulators to balance the current in the plurality of
17 interleaved buck converter circuits.

1 55. (New) A DC to DC switching circuit for controlling
2 power switching devices in a DC to DC converter having a
3 plurality of buck converter circuits operating into a common
4 load, comprising:

5 a plurality of pulse width modulators each controlling power
6 switching devices of one of the plurality of interleaved buck
7 converter circuits, the operation of the pulse width modulators
8 and the buck converter circuits being interleaved;

9 a feedback circuit responsive to a voltage across the common
10 load;

11 control circuits responsive to the feedback circuit and a
12 commanded output voltage to control a nominal duty cycle of the
13 plurality of buck converter circuits, the control circuits also
14 adjusting a relative duty cycle of the plurality of buck
15 converter circuits to balance the current in the buck converter
16 circuits.

1 56. (New) A circuit for a DC to DC converter having a
2 plurality of buck converter circuits operating into a common
3 load, comprising:

4 a plurality of pulse width modulators each controlling power
5 switching devices of one of the plurality of buck converter
6 circuits, the pulse width modulators being driven by a common
7 oscillator signal so that the operation of the pulse width
8 modulators is interleaved;

9 control circuits for adjusting a nominal duty cycle of the
10 plurality of interleaved buck converter circuits to control a
11 voltage on the common load, and for adjusting a relative duty
12 cycle of the plurality of buck converter circuits to balance the
13 current in the converter circuits.

1 57. (New) A DC to DC switching circuit for controlling
2 power switching devices in a DC to DC converter having first and
3 second interleaved buck converter circuits operating into a
4 common load, comprising:

5 a first pulse width modulator controlling the power
6 switching devices of the first buck converter circuit;

7 a second pulse width modulator controlling the power
8 switching devices of the second buck converter circuit;

9 a feedback circuit responsive to the voltage across the
10 common load;

11 control circuits for controlling the first and second pulse
12 width modulators responsive to the feedback circuit;

13 the control circuits also being responsive to current
14 measurements through the first buck converter circuit and the

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15 second buck converter circuit for adjusting the relative duty
16 cycle of the first and second buck converter circuits.


CONCLUSION

In view of the amendments and remarks made above, it is respectfully submitted that pending claims 1-22, 24-32 and 34-57 are in condition for allowance, and such action is respectfully solicited.

Respectfully submitted,

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Dated: October 10, 2001




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10/10/01

Date